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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,686	07/07/2003	Jean-Pierre Schoellkopf	S1022.81020US00	7411
23628	7590	10/19/2007		
WOLF GREENFIELD & SACKS, P.C. 600 ATLANTIC AVENUE BOSTON, MA 02210-2206			EXAMINER NADAV, ORI	
			ART UNIT	PAPER NUMBER
			2811	
			MAIL DATE	DELIVERY MODE
			10/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 10/614,686	Applicant(s) SCHOELLKOPF, JEAN-PIERRE	
	Examiner Ori Nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 September 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 1-6 and 12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7-11 and 13-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7-8, 11 and 13-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support for a circuit comprising insulating portions covering the edges of the metal regions of determined pairs, wherein the facing edges of at least one pair of the metal regions not being covered by the insulating portions, as recite in claim 7, since the insulating portions covering all the edges of the metal regions of determined pairs, as depicted in figure 1D.

There is no adequate description in the disclosure for the claimed limitations of "at least one insulating portion covering the facing edges of at least one first pair of the pairs of metal regions so as to encode at least one first bit; and metal portions that cover the facing edges and connect at least one second pair of the pairs of metal regions so as to encode at least one second bit having an opposite binary value with respect to the first bit", as recited in claim 11.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-8, 11 and 13-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of "at least one insulating portion covering the facing edges of at least one first pair of the pairs of metal regions so as to encode at least one first bit; and metal portions that cover the facing edges and connect at least one second pair of the pairs of metal regions so as to encode at least one second bit having an opposite binary value with respect to the first bit", as recited in claim 11, are unclear as to how an insulating portion encodes at least one first bit and how metal portions encode at least one second bit.

The claimed limitations of "each of the insulating portions being interposed between the facing edges of the metal regions of a determined pair and a covering one of the metal portions that is associated with the determined pair", as recited in claim 7, means that each of the insulating portions is interposed between element A (the facing edges of the metal regions of a determined pair) and element B (a covering one of the metal portions that is associated with the determined pair). It is unclear which element is the "a covering one of the metal portions".

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7-11 and 13-17, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (5,106,773).

Regarding claims 7-10, Chen et al. teach in figure 12 and related text an integrated circuit adapted to specific needs, comprising a stack of insulating layers 56, 66, 84, each layer being associated with a determined metallization level metal areas of the last and uppermost metallization level forming electric contacts of the integrated circuit, the integrated circuit comprising:

pairs of metal regions 26 of the penultimate metallization level having a facing edge and connected to components of the integrated circuit;

insulating portions 76 covering the facing edges of the metal regions of determined pairs according to the specific needs, and not covering the facing edges (located on the left side and figure 13) of the metal regions of at least one pair other than the determined pairs, and

metal portions 27 of the last metallization level which cover the facing edges of the metal regions of all of the pairs of metal regions, the metal portions connecting the metal regions 26 of the at least one pair other than the determined pairs and not connecting the metal regions of the determined pairs, each of the insulating portions 76 being interposed between the facing edges of the metal regions of a determined pair

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and a covering one of the metal portions that is associated with the determined pair,
and

a passivation layer 84 covering the metal portions.

Regarding claims 11 and 13-15, Chen et al. teach in figure 12 and related text an integrated circuit adapted to specific needs, comprising:

pairs of metal regions 26 formed in a metallization level and having facing edges;

at least one insulating portion 76 covering the facing edges of at least one first pair of the pairs of metal regions so as to encode at least one first bit and

metal portions 27 that cover the facing edges and connect at least one second pair of the pairs of metal regions so as to encode at least one second bit having an opposite binary value with respect to the first bit having the metal portions being formed in an uppermost metallization level of the integrated circuit, and

a passivation layer covering the metal portions,

wherein the integrated circuit is adapted to specific needs, and

wherein the pairs of metal regions are formed in a penultimate metallization level of the integrated circuit.

Regarding claims 16-17, the integrated circuit of prior art's device encodes a code having a plurality of bits, each bit being encoded by whether or not a pair of the metal regions is connected, wherein the integrated circuit hinders detection of the code by visual methods.

Response to Arguments

Applicant's arguments with respect to claims 7-11 and 13-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-D are cited as being related to antifuse structures.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized, cursive script.

O.N.
10/18/07

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800